Technical Consideration for Downsizing Crystal Design

With rapid development of modulization or miniature device, engineers may face the challenges to re-design the circuit with smaller size components. For the transition to small package crystals, not only frequency range, tolerance and load capacitance have to be compatible, the following factors are needed to be considered otherwise it would lead to have matching and reliability issue.

Frequency Limit

The typical AT-cut crystal resonator frequency is determined by the quartz blank thickness (inverse proportionality), it follows the relationship:

$$t = \frac{1.67}{f}$$

where:

t = Thickness in mm
1.67 = Frequency constant for AT-cut crystal
f = Frequency in MHz

Another design rule of the quartz blank is the length/thickness ratio, in general the ratio will be 10X ~ 20X, it helps to suppress the unwanted vibration modes. These two factors affect the low frequency margin for small package crystals, it's because the downsizing will limit the internal cavity, or the crystal blank would hit the cavity easily and causing reliability issues. Take 3225SX 8MHz as an example, user cannot change to a smaller design with same frequency it's because 8MHz blank is already the lowest limit for 3225SX package. If downsizing is essential, user have to pick a higher frequency in new design.

ESR (Equivalent Series Resistance)

With the same frequency range, crystal with smaller package will have a higher ESR value, it is recommended to review the circuit negative resistance (-R) margin, and check if the current design is good enough for fitting a small package crystal. Take 8MHz crystal as an example:

	5032SX 8MHz	3225SX 8MHz
Max ESR	150 Ohm	500 Ohm
Circuit negative resistance (-R)	-3200 Ohm	-3200 Ohm
Min -R recommendation	-3000 Ohm	-4000 Ohm
Safe design?	**Risk-free**	**Risky**

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If the circuit only has -3200Ohm -R, it is acceptable for utilizing 5032SX 8MHz because it's within the recommendation. Using 322SX 8MHz will be insufficient -R margin, as a result user may have occasional unstable oscillation in mass production.

TS (Trim Sensitivity)

TS defines how much frequency can be pulled according to the difference in load capacitance, it is expressed in following equation.

$$TS\ (ppm/pF) = \frac{C1 \times 10^3}{2(C0 + CL)^2}$$

Changing the crystal size means the quartz blank will be different, the parameters like shunt capacitance (C0) and motional capacitance (C1) would vary and hence the outcome frequency shall be different. Engineers have to review the error budget for the circuit, it will be critical for telecom. and IoT application. Below is an example.

	Crystal @TS=10ppm/pF	Crystal @TS=20ppm/pF
Tolerance at Room Temperature	10ppm	10ppm
Tolerance over Temperature	20ppm	20ppm
Ageing for 1st year	5ppm	5ppm
Component tolerance (=2pF x **Ts** of Crystal)	20ppm	40ppm
Measurement error (=0.4pF x **Ts** of Crystal)	4ppm	8ppm
Total frequency allowance	**59ppm**	**83ppm**

For the above reasons, in order to avoid these risk factors from downsizing the crystals, it is recommended design engineers to provide the new design to crystal manufacturer and conduct a matching service.

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