Crystal Drive Power Measurement

Crystal drive power is the amount of power dissipated in the crystal during oscillation. It is a vector product of the oscillation voltage and current through the crystal. Design engineer must ensure that the drive power does not exceed the maximum power rating of the crystal being used. Overstressing the crystal by excessive power may cause unnoticeable micro damage to the crystal, which may degrade its long term reliability.

Crystal Drive level is somewhat a less important parameter in old days, and often been overlooked. When SMD crystal package becomes smaller and smaller nowadays, this parameter becomes important and must be carefully characterized during circuit design.

The measurement setup for a typical Pierce-gate oscillator is shown in figure 1 to 3. A high frequency current probe is being used to measure the current through the crystal.

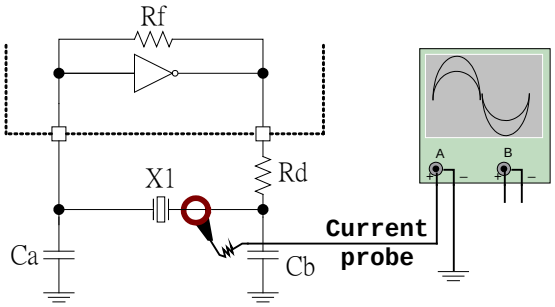

Figure 1

The drive power of the crystal can be represented by:

$$\text{Power} = \text{Id}^2 \cdot \text{RL} \qquad (1)$$

Since,

$$\text{RL} = \text{Rs}\left(1 + \frac{\text{C0}}{\text{CL}}\right)^2 \qquad (2)$$

Put (2) into (1), then,

$$\text{Power} = \text{Id}^2 \cdot \text{Rs}\left(1 + \frac{\text{C0}}{\text{CL}}\right)^2 \qquad (3)$$

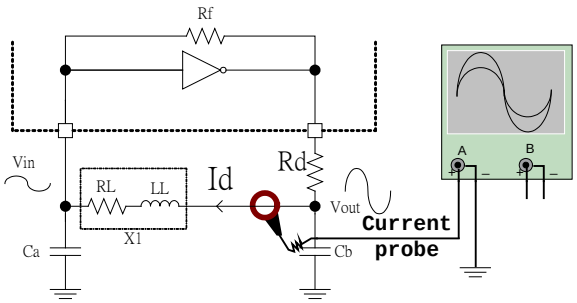

Figure 2

where,

Id = measured rms current through the crystal X1
Rs = equivalent series resistance of the crystal at series resonance
RL = equivalent series resistance of the crystal at load resonance
C0 = shunt capacitance of the crystal
CL = equivalent load capacitance of the oscillator circuit

From the equation (3), it can be seen that the drive power also depends on the crystal parameters Rs, C0 and CL as well.

The maximum drive power rating for most SMD crystal nowadays ranges from 100 to 200uW approximately. In any case if the measured drive power exceeds the maximum rating, circuit modification for reducing the power is recommended. There are two typical methods:

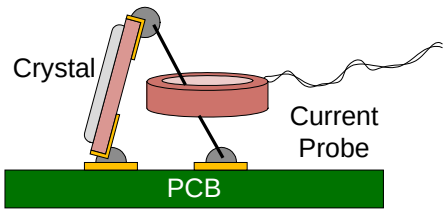

Figure 3

I. By adding a damping resistor Rd with initial value equals to the reactance of Cb:

$$\text{Rd} = \frac{1}{2 \cdot \pi \cdot \text{FL} \cdot \text{Cb}} \qquad (4)$$

By iterating the value of Rd and re-measuring the current Id, the drive power could be controlled to an optimum value without exceeding the maximum rating of the crystal.

II. By reducing Ca and Cb:

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The equivalent load capacitance (CL) would be reduced with smaller external capacitance Ca and Cb. From equation (2), it can be seen that the RL would be increased conversely, and therefore reducing the current through the crystal.

It should be noted that the drive power, the equivalent load capacitance (CL) and the negative resistance (-R) are interdependent. Whenever one parameter changed the other two would be affected as well.

For more information about negative resistance and load capacitance measurement, please refer to application note ANENG-XTL-0011 and 0012, or consult the crystal manufacturer.

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