Direct Impedance Method
For Load Resonant Measurement of Crystal

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Abstract **-- With today's hardware (Network Analyzers), the Direct Impedance Method provides better accuracy, convenience and at lower cost over other methods such as the Physical Load Capacitor method. However, a lot of crystal engineers still ask frequently, "Where is the Physical Load Capacitor?"**

This paper addresses how and why the Direct Impedance Method is better than the other measurement methods.

I. HISTORICAL BACKGROUND OF DIFFERENT MEASUREMENT METHODS

Due to the relatively low impedance of Fs and Fr, Fs/Fr measurements have never been difficult with both the IEC 444 and EIA 512 configurations. The challenge lies in FL measurement, especially at low CL.

This paper focus in Load Resonant (FL) measurement.

The impedance of a crystal at FL is relatively high, and to measure high impedance with a 50-Ohm network analyzer requires both high stability and good accuracy of the measuring equipment. Traditionally, these requirements were either impractical or too costly. Hence, several methods for FL measurement were derived, such as Calculated Method, and Physical Load Capacitor Method. These methods are designed to measure a crystal at lower impedance level, thus hopefully, allowing equipment with lower accuracy to be used. This paper will discuss in detail the merits and drawbacks of these methods.

II. VARIOUS FL MEASUREMENT METHODS

A. Calculated Method

As described in the IEC 444 publications, the DUT (Device Under Test) is measured at about ±45 degree for its motional parameters, and then the FL is "Calculated" based on this ±45 degree data (see Figure 1).

The advantage of this method is that the DUT is measured at relatively low impedance, close to 25 Ohm. Hence, the requirement of software compensation for stray components in the test head is relatively simple.

The drawback of this method is that the DUT is not tested at its destined condition : i.e. not at the phase shift equal to the specified CL / FL. If the crystal behaves strictly according to its four component model, this method is acceptable. However, if the crystal is NON-Linear (not behaving as per the four component model [2], see Figure 2, and **Figure 3**) then, the FL measurement will not be accurate.

If you know already your DUT is a linear crystal, you may use this method to test it. However, in most case, you need a test method to tell you how good the DUT is, so this method is quite useless, unless you know the crystal is linear before testing.

A.1. Linearity of a crystal

- Circuit Application standpoint :
  As long as the crystal has a stable (repeatable), sharp impedance –frequency curve, and it functions properly in an oscillator, then it is a good crystal; whether it is linear, or not, is not a question. Non-linear crystal does not imply a bad crystal.
- Crystal Designer standpoint :
  The market trend is toward smaller crystals, such as the AT-strip crystal and SMD crystal. Unlike larger crystals with circular geometry, these are inherently more difficult to model using the four component method. However, the problem with measurement does not necessarily imply a bad crystal. Instead, we need some test method or system that can measure the crystal more accurately in spite of non-linearity, and provide more information, such as how serious a spurious mode is affecting the crystal performance over temperature.
- Crystal Measurement standpoint :
  The Calculated Method is not suitable for testing a non-linear crystal, because the degree of measurement accuracy depends on the crystal characteristics, which may vary significantly[2]. If there are other practical means of measurement, we should simply abandon the use of this method.

B. Physical Load Capacitor Method

As described in the IEC 444 standard, the basic concept of this method is to measure the crystal at its specified CL condition, by inserting an actual capacitor in series with the crystal and measuring both simultaneously (see Figure 4).

This is a good improvement over the Calculated Method, as no more estimation is done, while the Network Analyzer measures FL at relatively low impedance.

B.1. This method has been widely used and it seems to have the following advantages :

- Good "Repeatability" in FL, as compared to the Calculated Method;
- Correlation between different machines can be done easily by trimming the physical load capacitor. No need to change any software parameters: Simply keep a look up table between different customers / suppliers / machines / frequency / and test head configurations for the differences in CL;
- Measurement speed is good.

B.2. The well known disadvantage is :

- The Fr/Rr/Co values cannot be measured accurately in a one-pass test. The same DUT must be tested twice: With and without the physical load capacitor so as to get all parameters with reasonable accuracy. These measurements become more difficult when DLD and Spurious Mode measurements are made. ([1] IEC 444-6 : Both DLD measurements and Spurious measurements: are based on series measurements instead of load measurements) .

B.3. The problem with Physical Load Capacitor Method

If we look into the "Advantages" more closely, we may well ask: If this method is good enough for accurate measurement, then why are we still correlating with a look up table of CL ?

The answer is crystal clear, the method is not good enough, but we accept the habit because it ***seems*** that there is no other better choice.

The difficulty in getting accuracy in this method is :

- The impact of stray components (CX and CY in [2]) on accuracy is significant and difficult to compensate (as described in [2]);
- The IEC standard [1] defines an "ideal" test jig with minimal stray component (CX and CY). However, the "ideal" test jig is often impractical in mass volume / automation applications, and so "minimal stray" may be difficult to achieve. Also, a variable CL in the "ideal" test jig jeopardizes the "ideal" behavior of that jig due to excessive stray components.
- Many engineers have tried very hard to compensate for CX and CY to obtain an acceptable level, however in vain.
- To look into the issue in greater detail, the stray components may not be limited to CX and CY, it could have been a lumped circuit with LX and LY … That is why the correlation table that we use also involves frequency as a variable.

B.4. Major technical difficulties :

Both calibrating the Physical Load Capacitor and compensating for the stray capacitance and inductance at the junction of the crystal and the capacitor remain largely unresolved.

C. Direct Impedance Method

From the circuit application standpoint, a circuit requiring FL at CL means that the crystal must behave, at the specified FL, as an inductor :

The impedance of DUT = - Impedance of CL.

This is the basic requirement, and whenever possible the crystal should be tested at exactly this condition without any estimation. The Direct Impedance Method is based on this basic principle.

C.1. Test Set up and Method

The test set up of the Direct Impedance Method is simple (see **Figure 5** and **Figure 6**) :

- The DUT is placed into a π-network test head.
- With the same hardware configuration according to IEC444 [1], measure Co, Fr, and Rr.
- The frequency of the frequency synthesizer is iterated to search for :

  the impedance of DUT = - impedance of CL.
- The other motional parameters L1 and C1 are then calculated based on the FL, Fr and Co.

C.2. Major Advantage

- Measure the crystal at its destined CL condition. No more estimation is done, so that even if the crystal is non-linear, it does not matter.
- Does not have to calibrate CX, CY (or LX, LY, etc.) in the presence of an unknown physical CL. This would allow accuracy and reproducibility, instead of only repeatability.
- Fr/Fs/FL/Rr/Rs all measured at one time, making DLD and spurious response measurement much easier and more accurate.

The following discussion [section III] will present the test data of Repeatability, Reproducibility and Accuracy in detail.

C.3. Other considerations

a) Software calibration and stray component compensation :

The IEC 444 standard does not require explicitly stray component compensation and calibration with software techniques but rather relies on a perfect test head. Without proper software compensation, the IEC 444 standard is limited to measuring at low impedance with the ideal test head.

However, such a test head with minimal stray components is impractical in mass volume operations. That is why most practical measurement systems are already implemented to some extent with software techniques to compensate stray reactive components.

The Direct Impedance Measurement Method requires a more comprehensive model of the π-head and more extensive

mathematical computations, which fortunately, are practical with the speed and cost of today's computers / network analyzers. This must be done properly, otherwise the system will not be able to measure high impedance with good Repeatability, Reproducibility and Accuracy.

b) Drive level

When measuring FL, the voltage amplitude required in the Direct Impedance Method is much larger compared to the other methods using the same hardware set up.

- Luckily, when measuring Fr/Fs, the same drive level range can be achieved compared with other methods. Hence, DLD (Drive Level Dependency) and Spurious Ratio tests can be done accurately, providing a safe guard on extremely poor crystals.
- The accuracy of the Drive Level with the passive measurement (both IEC444 and EIA512 standards) has always been subject to question: Within a typical one-second test, most of the iteration search is not applying the target drive power to the DUT. Until the last few readings, it may be possible to exert the target drive power, but these readings take just a few milliseconds or fractions of a millis econd. This is the same for all the above mentioned test methods.
- With the addition of a commercially available power amplifier, costing in the range of a few hundreds USD to over a thousand, the practical drive level of this method can go up to >400 micro-Watt at say CL=20 pF, 20MHz. This is an acceptable range for today's crystals --- especially when the size is getting smaller and the drive level of the application circuit is getting lower.

  So, in the case of serious research work, a little higher cost helps to overcome this problem. When cost is a concern, then precautions must be taken to use DLD and Spurious tests as a safe guard against bad crystals.

c) Measurement Speed

With today's hardware (network analyzers and computers that are high speed and available at acceptable cost), measurement speed relies on the programming techniques and the iterative search algorithms. The various methods described herein do not have big differences in speed, but of course programming techniques and the iterative search algorithm matter.

The measurement data in Section III are all obtained within 0.5 seconds utilizing a Pentium II 300 MHz computer and network analyzers that are commercially available at reasonable cost.

D. Other Methods (Variations/Combinations Of The Above Methods)

D.1. Measured Method

This method is applicable to CI meters using an oscillator configuration. The accuracy of this implementation is inferior to the IEC444 (and EIA512) methods, and no further development in this area has been made.

This method is also commonly used as a supplement to the "Physical load capacitor" Method where the physical load capacitor is always slightly different than the target CL. This supplement defeats the advantage of the Physical load capacitor method of measuring the DUT at the exact phase shift condition of the specified CL.

Detailed error analysis on this method is complicated as it depends on the DUT' s linearity and Trim Sensitivity.

D.2. Curve Fit implementation

Some equipment manufacturers make use of the Curve Fit algorithm suggested in the IEC standard [1] (Admittance Circle). This method is a software "iterative search" and does not address the measurement problem of Crystal Linearity property, nor does it address the stray component compensation issue.

Hence, the "Admittance Circle" method does not help to resolve the repeatability and accuracy problem.

D.3. VCO-PLL Implementation

Some equipment manufacturers put the DUT into a PLL (Phase Locked Loop) comprised of a VCO (Voltage Controlled Oscillator) as shown in Figure 7.

The primary objective is to improve speed, and cut down hardware cost.

We suspect that this configuration has the difficulty of :

- A perfect control loop design that can accommodate a DUT of unknown parameters before test (including, but not limited to: ESR, pullability, spurious response of the unknown crystal under test), so that the loop is stable enough to allow the measurement subsystem to do parametric readings with accuracy. The stabilization time of the loop also affects measurement speed.
- Usually, the basic control parameter of the PLL loop is Phase. More work will have to be done to correlate the phase measurement resolution/ accuracy to the CL / TS accuracy.
- The difficulty in applying a software compensation technique for stray components (CX, CY, and not to forget : LX, LY …) for a wide frequency range in this rather complicated environment.

III. COMPARISON TEST DATA WITH DIFFERENT HARDWARE CONFIGURATIONS

Test data using the same Direct Impedance Measurement Method using different network analyzers, different test heads, different frequencies and different CL are presented to verify the result of a proper implementation of the test method.

A. Experiment Matrix

For repeatability and reproducibility test, we use the Direct Impedance Measurement Method equipped with:

- 2 different Network Analyzers: Hewlett Packard E5100A, and Kolinker KH1200. Both are equipped with internal frequency reference, warmed up, and calibrated.
- 4 different kind of Test Jigs #1 to #4 as per
- Figure 8, including an IEC compatible Jig and 3 other jigs suitable for volumn production;
- One crystal of 11.150MHz HC49US, tested 1400 times on each of the above combinations of Network Analyzers and test jigs, for Fs and FL at CL=10, 20 and 30 pF.

For accuracy test, the above test data are used with the addition of :

- Using the Physical Load Capacitor Method, and a Fixed Physical CL at 8.725pF. No software compensation on head parameters was used.
- Using the Physical Load Capacitor Method, and a Variable Physical CL tuned to 10pF. No software compensation on head parameters was used.

B. Raw Data

As the data volumn is very large, the mean and standard deviation of each group of data is presented in Figure 9 to Figure 11.

For repeatability and reproducibility, Figure 9 and Figure 10Figure 10 show that the repeatability and reproducibility of the Direct Impedance Method is good : well within |0.2pF| for crystal with Ts as large as 30 to 40 ppm/pF.

For accuracy, Figure 11 shows that the method yields good accuracy (well within |0.2pF|) when compared with an ideal test jig (small stray component). But the physical load capacitor method with an non-ideal test jig (variable load capacitor, large stray component) is not comparable.

C. Comment on the Experiment

The above data shows that the Direct Impedance Method worth more attention and effort to be focused because of its repeatability, reproducibility and accuracy with different hardware configurations.

However, more experiment should be done to verify:

- Error due to different frequency standards;
- Error due to different crystal samples : overtones, deliberately chosen non-linear crystals etc.

IV. CONCLUSION

Based on the above conceptual and experimental data, we propose that more effort should be spent on the Direct Impedance Measurement Method with the goal of possibly further enhancing the IEC444 and EIA512 measurement standards.

The above discussion focuses on the accuracy of FL measurement because this is the greatest headache in the crystal industry. We also have to be reminded that the method also gives accurate results for Fs, Fr, Co and ESR. This means that in a one-pass test, we can test all crystal parameters including DLD, spurious mode, Q, etc. without the need to insert or change any load capacitor. Equipment utilizing this method is now commercially available providing accurate measurement of all crystal parameters with superb user friendliness and at low cost.

A. Advantages

- Good Accuracy and Reproducibility for FL.
- Measure the crystal at its destined CL condition without estimation, so that even if the crystal is non-linear, measurement repeatability and reproducibility is not compromised.
- Measure all parameters in one test, so that DLD Spurious mode measurements are more convenient.
- Less unknown stray components to be calibrated. This would allow accuracy and reproducibility, instead of only repeatability.

B. Precautions

When using lower cost equipment with Direct Impedance measurement that cannot measure FL at the target drive level, we recommend the use of DLD and spurious test as a safe guard against possible extreme situations.

C. Future work to be done

Before we could formally present this method as an international standard, we will have to challenge ourselves :

C.1. Non-ideal test head

More work needs to be done so as to identify the error relationship with the "non-ideal" test head stray parameters, so that we can know more precisely how "Non-ideal" a test head can be.

C.2. Resolution/Accuracy and Speed

More work has to be done so as to identify the optimal/feasible relationship of resolution in frequency and speed.

C.3. More test data on :

- different Frequencies,
- different Cut angle,
- more samples, and,
- connect the same external time base to all hardware for the experiment.

C.4. Drive Level Study

The following studies would require extensive work to be done :

a) Iterative Search

This intrinsic nature of passive measurement affects the drive level accuracy : Does it matter or does it not ?

b) The physical meaning of Linearity

Linearity relates to spurious response, but is Linearity also related to the size and structure of the crystal device, or

what else ? Is it possible to define quantified limits for different measurement methods ?

C.5. π- Network values

Should the termination impedance of the IEC 444 be changed to higher values ?

REFERENCES

[1] IEC Publication 444-1 to 444-6 : Measurement of quartz crystal unit parameters by zero phase technique in a π-network.

[2] Dwane Rose, Saunders and Associates, Inc., Load Resonant Measurements of Quartz Crystals, http://www.saunders-assoc.com/paper/paper.html .

ACKNOWELDGEMENT

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Figure 1 : The Calculated Method

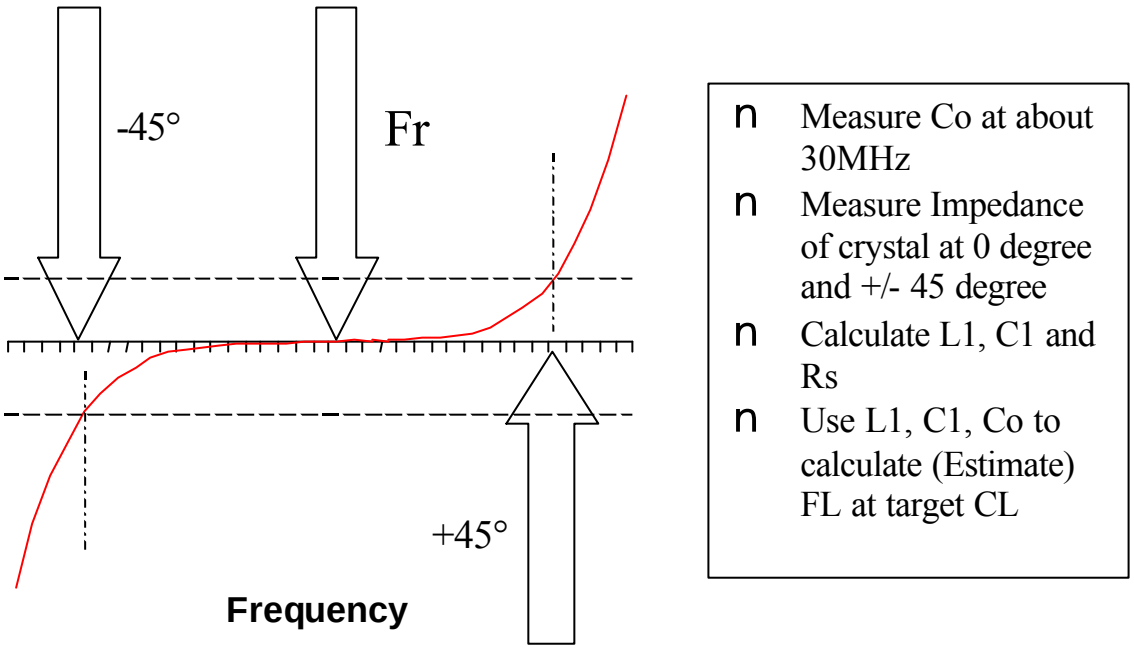


Figure 2 : The Four component model

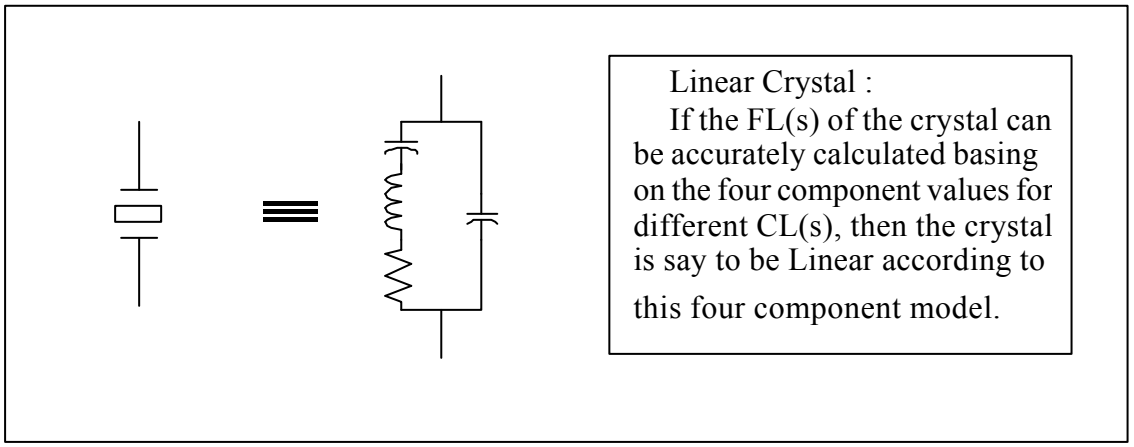


Figure 3 : Impedance of Linear and Non-Linear Crystals

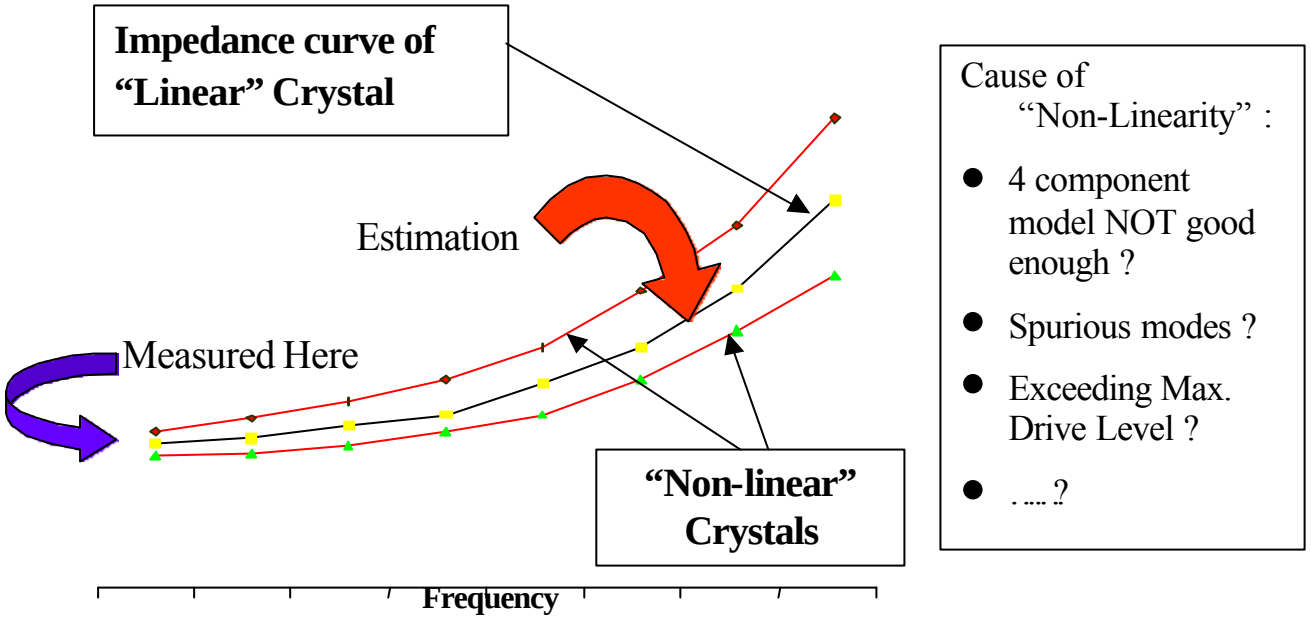


Figure 4: Physical Load Capacitor Method

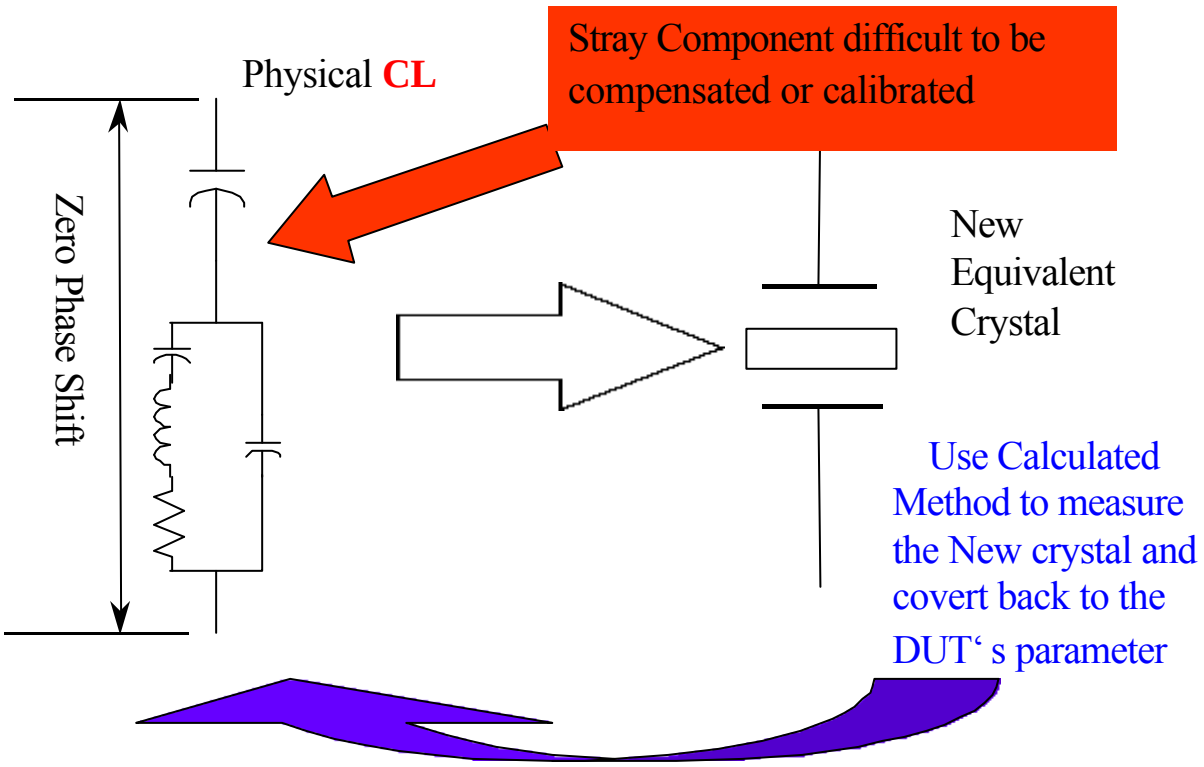


Figure 5 : Direct Impedance Measurement Method

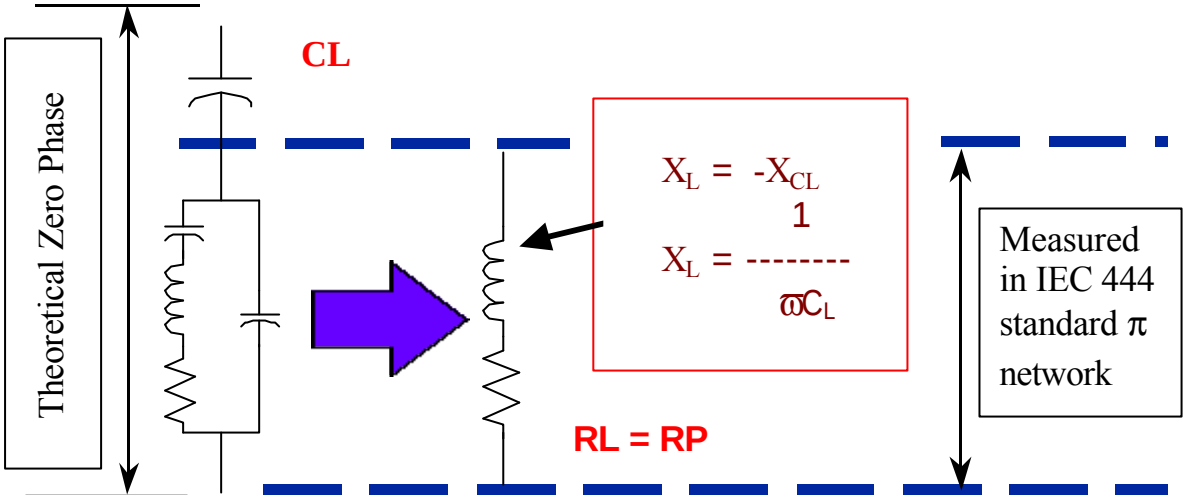


Figure 6 : Direct Impedance Measurement Impedance Map

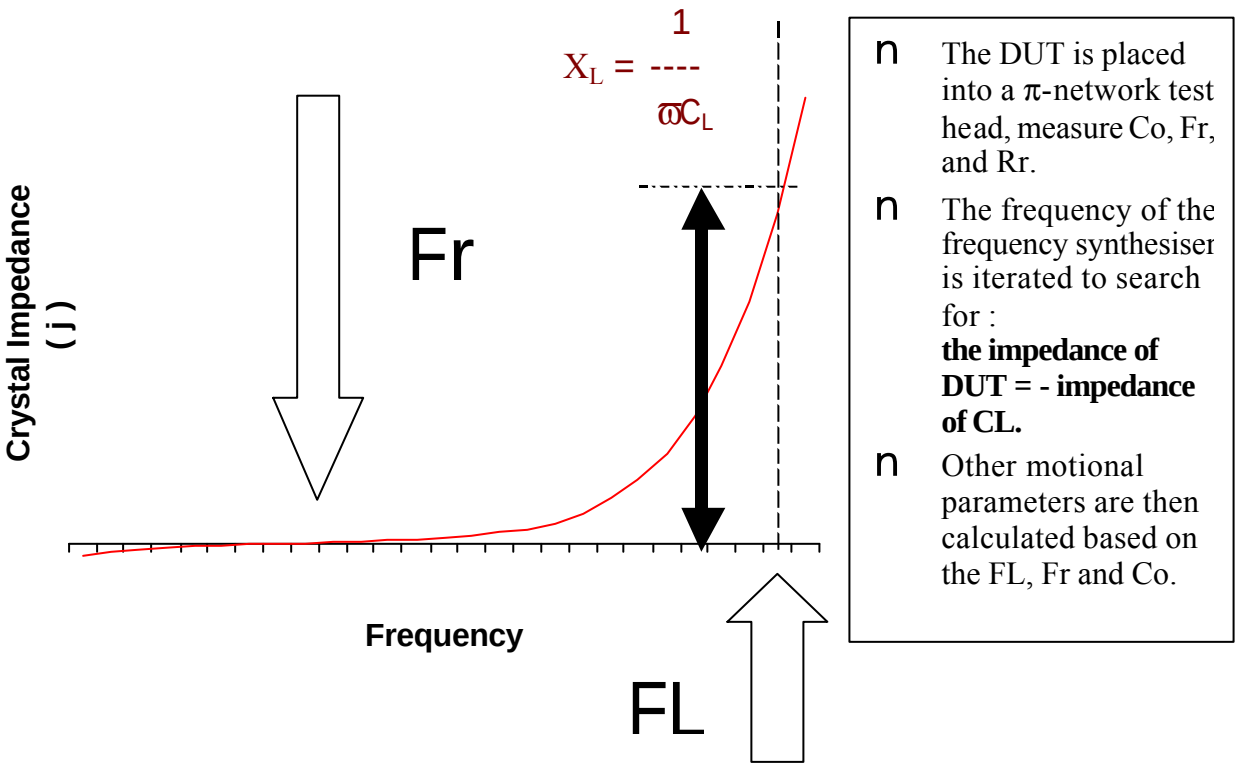


Figure 7 : VCO-PLL Configuration

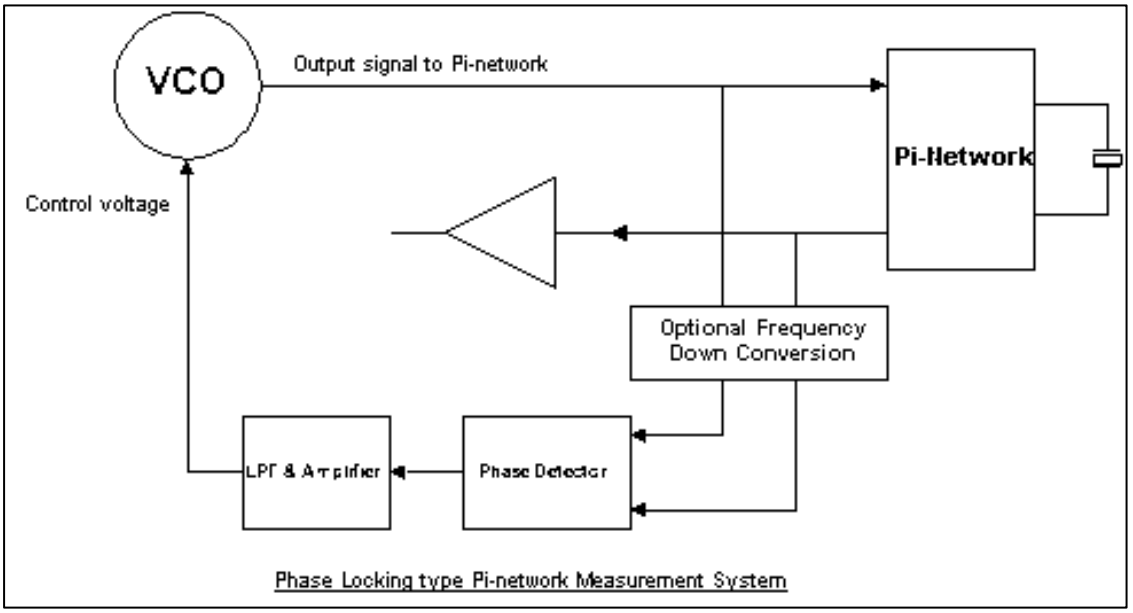
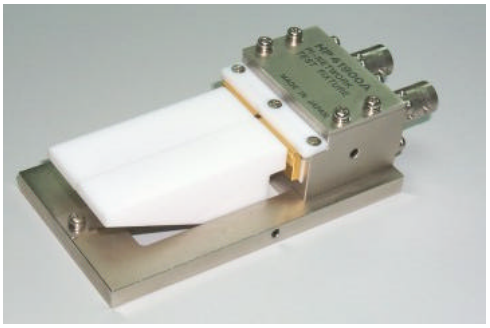
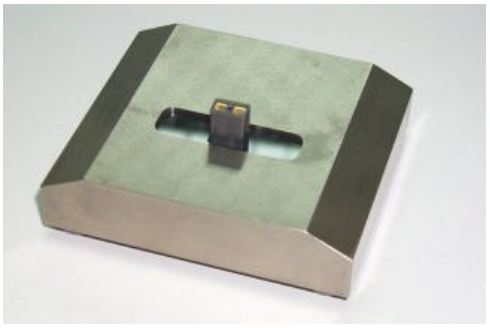


Figure 8 : Test Jigs

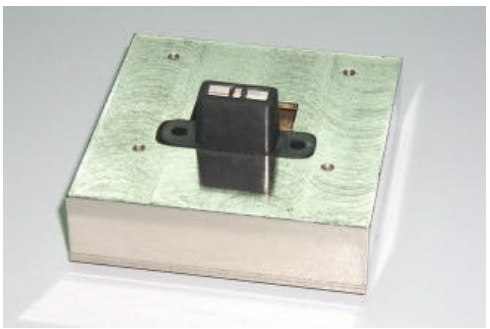
Test Jig #1 : HP41900A



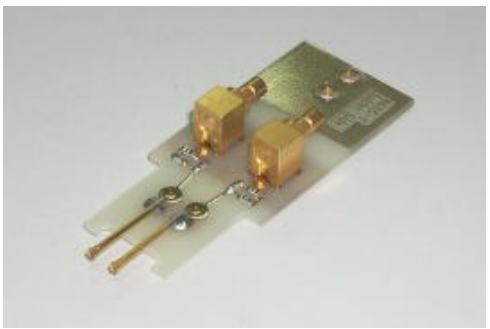
Test Jig #2 : Kolinker 88012000-07-021



Test Jig #3 : Kolinker 8801200-07-020



Test Jig #4 : Kolinker 8803288-16-000



Note : The above Jigs have different stray component configurations.

Figure 9 : Error between different Hardware Configurations

Mean of 1400 readings [ppm]	Network Analyser	Different Test Jig				Max error [ppm]	Max error in CL [pF]
		#1 Jig	#2 Jig	#3 Jig	#4 Jig		
Fs	E5100A	-310.78	-310.72	-310.62	-310.66	0.90	N/A
	KH1200	-310.70	-311.38	-311.37	-311.52		
FL at CL=8.725pF	E5100A	130.73	130.52	131.43	131.22	0.91	0.02
(Ts = 40ppm/pF)	KH1200	131.22	131.17	131.41	131.36		
FL at CL=10pF	E5100A	86.98	86.11	87.39	87.39	1.28	0.04
(Ts = 30ppm/pF)	KH1200	87.11	87.07	86.94	87.14		
FL at CL=20pF	E5100A	-87.44	-87.71	-86.99	-87.30	0.77	0.07
(Ts = 10ppm/pF)	KH1200	-86.94	-87.61	-87.52	-87.80		
FL at CL=30pF	E5100A	-155.59	-155.70	-155.19	-155.49	0.93	0.18
(Ts = 5ppm/pF)	KH1200	-155.67	-155.91	-155.21	-156.12		

Figure 10 : Repeatability (spread) between different Hardware Configurations

Standard Deviation of 1400 readings	Network Analyser	Different Test Jig			
		#1 Jig	#2 Jig	#3 Jig	#4 Jig
Fs	E5100A	0.037	0.027	0.025	0.021
	KH1200	0.028	0.018	0.022	0.029
FL at CL=10pF	E5100A	0.174	0.167	0.166	0.170
	KH1200	0.340	0.333	0.323	0.333
FL at CL=20pF	E5100A	0.018	0.014	0.014	0.010
	KH1200	0.173	0.186	0.182	0.189
FL at CL=30pF	E5100A	0.021	0.017	0.016	0.012
	KH1200	0.130	0.140	0.139	0.136

Figure 11 : Error between Physical Load Capacitor Method

Mean of 1400 readings [ppm]	Network Analyser	Different Test Jig				Note A	Note B
		#1 Jig	#2 Jig	#3 Jig	#4 Jig		
Fs	E5100A	-310.78	-310.72	-310.62	-310.66		
	KH1200	-310.70	-311.38	-311.37	-311.52		
FL at CL=8.725pF	E5100A	130.73	130.52	131.43	131.22		123.98
(Ts = 40ppm/pF)	KH1200	131.22	131.17	131.41	131.36		125.50
FL at CL=10pF	E5100A	86.98	86.11	87.39	87.39	64.02	
(Ts = 30ppm/pF)	KH1200	87.11	87.07	86.94	87.14	65.58	

Note A : CL=10pF : obtained by a variable capacitor (significant stray components), tuned and checked according to IEC 444 procedures, but without any further software compensation on stray components. Error is large (13 / 30 = 0.5 pF) due to uncompensated stray components.

Note B : CL=8.725pF : obtained by fixed capacitor (small / insignificant stray components), tuned and checked according to ICE444 procedures, without any further software compensation on stray components. Error is small (7 / 40 = < 0.2 pF) due to less uncompen sated stray components.